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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,768	LIAW ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 46-67 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 46-49, 51-54 and 56-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakase et al PN 6,392,897.

In regards to claim 46: Nakase et al teaches (Figure 9) a memory module (20b), comprising: a first circuit board (9 or alternatively 2) including a first conductive trace (11a) disposed on a surface of the first circuit board; a first connector (15a) including at least one contact (15a) connected to the first conductive trace (11a), wherein the first connector is for removable connecting the first circuit board (9) to a second circuit board (2); and a first capacitor (18a) including: one capacitor electrode connected to the first connector at a junction (5e) where the contact connects to the first conductive trace (bottom electrode); and another capacitor electrode coupled to a node that is at a supply potential (19a Ground).

In regards to claim 47: Nakase et al teaches edge contacts (21a and 21b).

In regards to claim 48: Nakase et al teaches an additional set of edge contacts on another surface substantially parallel to the surface (15c coupling 21b).

In regards to claim 49: Nakase et al teaches the contact is a conductive pad disposed on the surface and proximate to an edge of the surface of the first circuit board (21a and 21b when 2 is taken as the first circuit board).

In regards to claim 51: Nakase teaches the first circuit board is a mother board and the second circuit board is a daughter board (when 2 is taken as the first circuit board).

In regards to claim 52: Nakase teaches one of the capacitor electrodes being a conductive pad on the circuit board.

In regards to claim 53: Nakase teaches the supply potential being ground.

In regards to claim 54: Nakase teaches a conductive ground plane (Figure 10 item 19b).

In regards to claim 56: Nakase teaches different impedance values.

In regards to claim 57: Nakase teaches the capacitor is for impedance matching.

In regards to claim 58: Nakase teaches a plurality of memory devices (3)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 50 and 62-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakase et al PN 6,392,897 in view of Shepherd PN 4,781,624.

In regards to claim 50: Nakase teaches the capacitor coupling as described above. Nakase teaches a slotted board as opposed to pin connectors. Shepherd teaches a first circuit board (14 or alternatively 21) including a first conductive trace (such as for example 24) disposed on a surface of the first circuit board; a first connector including at least one contact connected (3) to the first conductive trace, wherein the first connector is for removably connecting the first circuit board to a second circuit board (21 or alternatively 14); and a first capacitor including (30): one capacitor electrode connected to the first connector at a junction where the contact connects to the first conductive trace (at 29); and another capacitor electrode coupled to a node that is at a supply potential (one capacitor 30 is attached to VCC the other is attached to ground). Shepherds connectors are pins. Shepherd does not however teach the circuit is a memory module. It would have been obvious to support Nakase's capacitor coupling in a system that uses DIP pins or alternatively make Shepherd's circuit be a memory module because this would have prevented limiting the usable structures.

In regards to claim 62: Nakase teaches a capacitor attached to the inserted circuit board for impedance matching as described above. Shepherd teaches a capacitor attached to the base circuit board for noise filtering as described above. It would have been obvious to include a capacitor on both circuit boards because this would have allowed for impedance matching and noise filtering.

In regards to claim 63: Both Shepherd and Nakase teach motherboard and daughter boards.

In regards to claim 64: Nakase teaches the circuit boards being substantially orthogonal (perpendicular).

In regards to claim 65: Shepherd teaches the capacitor is for noise reduction. Shepherd does not teach the capacitor affects impedance. Nakase teaches (figure 20 and Column 3 lines 34 to Column 4 line 12) that all capacitors attached affect the impedance and the capacitance values chosen should be for optimum impedance matching. It would have been obvious to chose a capacitance that provides impedance matching as the second capacitor because this would have provided for minimum impedance differential thus minimized signal reflection and thus minimized noise which by the way is the purpose of Shepherd.

In regards to claim 66: Nakase and Shepherd both teach conductive pads. Nakase teaches edge connectors.

In regards to claim 67: Nakase teaches right angle turns at the ends of the conductive trace.

6. Claims 55 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakase et al PN 6,392,897 in view of Burger et al PN 4,788,766.

In regards to claim 55: Nakase teaches the circuit board with signal traces and a ground plane. Nakase is silent upon the existence of a dielectric disposed between the signal traces and ground plane. Burger expressly teaches a dielectric between the signal traces and the ground plane. It would have been obvious to include a dielectric between the signal traces and ground plane because this would have prevented the circuits from shorting out.

In regards to claim 59: Nakase teaches signal traces. Nakase is silent as to the type of signal traces. Burger teaches multiple types of signal traces such as stripline and microstrip. It

would have been obvious to use microstrip as the trace because this is a standard type of signal trace.

7. Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakase et al PN 6,392,897 in view of Geiszler PN 3,359,510.

In regards to claim 60: Nakase teaches handling impedance matching. Nakase does not teach varying the width of the conductor for impedance matching. Geiszler teaches varying the width of a conductor for impedance matching. It would have been obvious to a person of ordinary skill in the art to use width varying for impedance matching because this would have allowed for handling microwave frequency.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
November 8, 2004

PAUL R. MYERS
PRIMARY EXAMINER